Exhibit 19

PC3200/PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM

Reference Design Specification

Revision 1.4

January 10, 2003

Contents

1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC3200 module, a 200-pin, 200 MHz clock (400 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate (DDR) DRAM Small Outline Dual In-Line Memory Module (DDR SDRAM SO-DIMMs). It also defines a slower version, PC2700, using 167 MHz clock (333 MT/s data rate) or PC2100, using 133 MHz clock (266 MT/s data rate) or PC1600, using 100 MHz clock (200 MT/s data rate) DDR SDRAMs. These DDR SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers or small form factor PCs. PC3200 DIMM modules use DDR400 devices.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for the supported maximum clock rate. Other designs are acceptable, and all Unbuffered SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

Attribute:	Values:	Notes:
SO-DIMM Organization	x 64, x 72	
SO-DIMM Dimensions (nominal)	31.75 mm high, 67.60 mm wide	
SO-DIMM Types Supported	Unbuffered, Unbuffered with PLL, Registered with PLL	
Pin Count	200	
SDRAMs Supported	64 Mb, 128 Mb, 256 Mb, 512 Mb, 1 Gb	
SDRAMs Device Widths Supported	x8, x16	
Capacity	32 MB, 64 MB, 128 MB, 256 MB, 512 MB, 1 GB	
Serial Presence Detect	Consistent with JEDEC Rev. 1.0	
Voltage Options	2.5 V V_{DD} 2.5 V $V_{DD}Q$ 2.6 V for V_{DD} PC3200 module only 2.6 V for $V_{DD}Q$ PC3200 module only 2.5 V to 3.3 V $V_{DD}SPD$	1
Interface	SSTL_2	
Note 1: $V_{DD}SPD$ is not tied to V_{DD} or $V_{DD}Q$ on the DDR SO-DIMM.		

Product Family Variations (Raw Cards)

Raw Card	Device Type	Module Bus Width	Device Width	Number of Devices	Physical Banks	Capacity
A	TSOP-II	x64	x16	8	2	256 MB to 1 GB
B	TSOP-II	x64	x8	8	1	256 MB to 1 GB
C	TSOP-II	x64	x16	4	1	128 to 512 MB
C	TSOP-II	x72	x16	5	1	128 to 512 MB

2. Environmental Requirements

PC3200/PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to +100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

CK(0:2)	Clock Inputs, positive line	3	DQ(0:63)	Data Input/Output	64
$\overline{CK}$(0:2)	Clock inputs, negative line	3	CB(7:0)	Data check bits Input/Output	8
CKE(0:1)	Clock Enables	2	DM(0:8)	Data Masks	9
$\overline{RAS}$	Row Address Strobe	1	DQS(0:8)	Data strobes	9
$\overline{CAS}$	Column Address Strobe	1			
$\overline{WE}$	Write Enable	1	V_{DD}	Core and I/O Power	33
$\overline{S}$(0:1)	Chip Selects	2	V_{SS}	Ground	33
A(0:9,11:13)	Address Inputs	13	V_{REF}	Input/Output Reference	2
A10/AP	Address Input/Autoprecharge	1	V_{DD}SPD	SPD Power	1
BA(0:1)	SDRAM Bank Address	2	V_{DD}ID	V_{DD}, V_{DD}Q level detection	1
SCL	Serial Presence Detect (SPD) Clock Input	1			
SDA	SPD Data Input/Output	1	TEST	Reserved for test equipment use	1
SA(0:2)	SPD address	3	DU	Reserved for future use	5
				Total:	**200**

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK2, $\overline{CK0}$ - $\overline{CK2}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	Input	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S0}$; Bank 1 is selected by $\overline{S1}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0 - BA1	Input	—	Selects which DDR SDRAM bank of four is activated.
A0 - A9, A11-A13 A10/AP	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	In/Out	—	Data Bit Input/Output pins.
CB0 - CB7	In/Out	—	Data Check Bit Input/Output pins. Not used on x64 modules.
DM0 - DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
DQS0 - DQS8	In/Out	—	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR SDRAMs and is sent at the leading edge of the data window. DQS8 is associated with check bits CB0-CB7, and is not used on x64 modules.
V_{DD}, V_{DD}SPD, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
V_{DD}ID	Out	—	Defines relationship of V_{DD} and V_{DD}Q. If V_{DD}ID is open, V_{DD} = V_{DD}Q; if V_{DD}ID is pulled to V_{SS}, $V_{DD} \neq V_{DD}$Q. This line should be pulled high through 10 KΩ on the host board.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.
SA0 - SA2	Input	—	Address pins used to select the Serial Presence Detect.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).

DDR SDRAM SO-DIMM Pinout

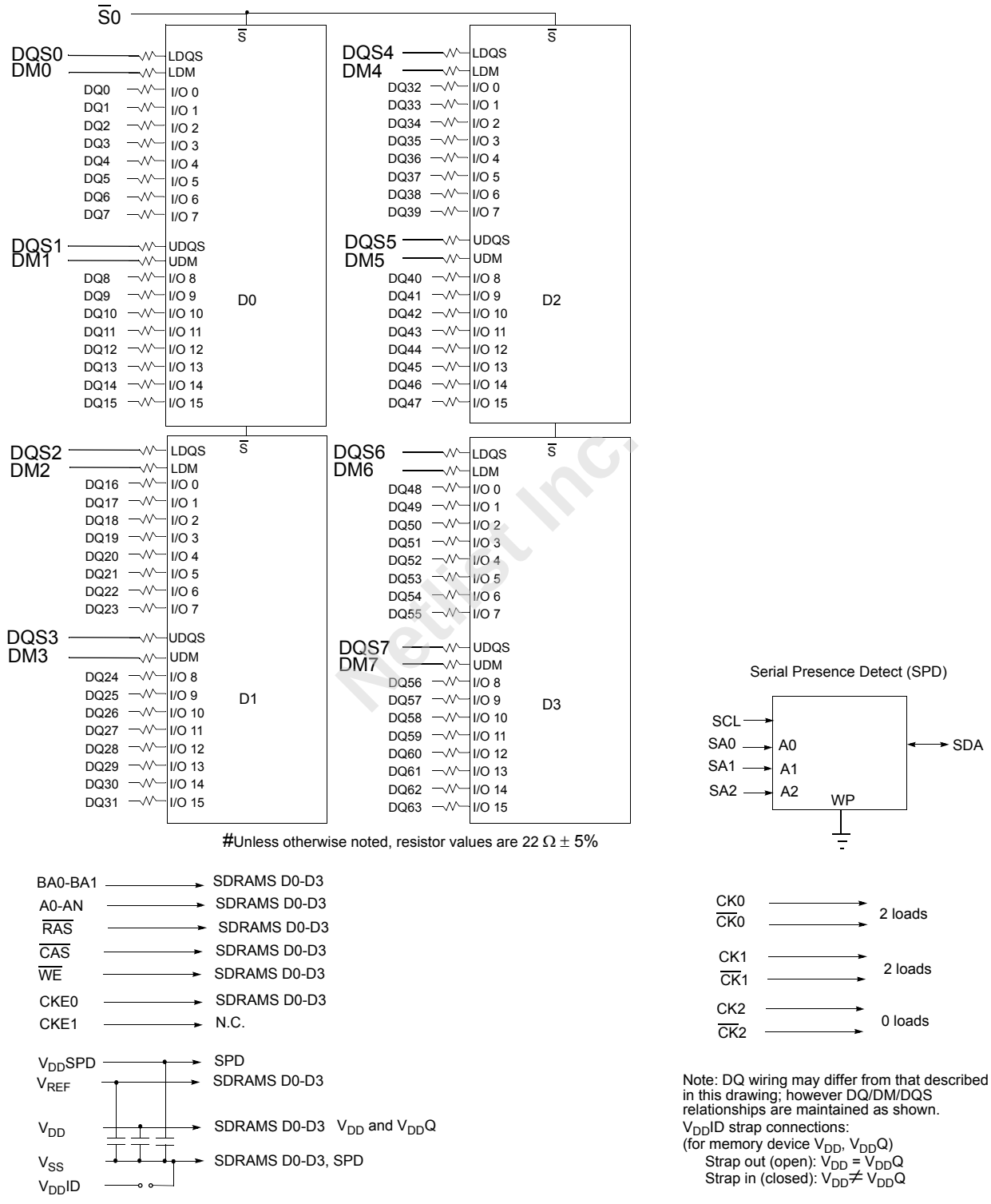
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V_{SS}	4	V_{SS}	53	DQ19	54	DQ23	103	V_{SS}	104	V_{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V_{DD}	156	V_{DD}
7	DQ1	8	DQ5	57	V_{DD}	58	V_{DD}	107	A5	108	A4	157	V_{DD}	158	$\overline{CK}1$
9	V_{DD}	10	V_{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V_{SS}	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V_{SS}	162	V_{SS}
13	DQ2	14	DQ6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ48	164	DQ52
15	V_{SS}	16	V_{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	$\overline{RAS}$	167	V_{DD}	168	V_{DD}
19	DQ8	20	DQ12	69	V_{DD}	70	V_{DD}	119	$\overline{WE}$	120	$\overline{CAS}$	169	DQS6	170	DM6
21	V_{DD}	22	V_{DD}	71	CB0	72	CB4	121	$\overline{S}0$	122	$\overline{S}1$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	A13	124	DU	173	V_{SS}	174	V_{SS}
25	DQS1	26	DM1	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	V_{DD}	180	V_{DD}
31	DQ11	32	DQ15	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ57	182	DQ61
33	V_{DD}	34	V_{DD}	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	V_{DD}	85	DU	86	DU ($\overline{RESET}$)	135	DQ34	136	DQ38	185	V_{SS}	186	V_{SS}
37	$\overline{CK}0$	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ58	188	DQ62
39	V_{SS}	40	V_{SS}	89	CK2	90	V_{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{CK}2$	92	V_{DD}	141	DQ40	142	DQ44	191	V_{DD}	192	V_{DD}
43	DQ17	44	DQ21	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA0
45	V_{DD}	46	V_{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	V_{DD}SPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V_{SS}	150	V_{SS}	199	V_{DD}ID	200	NC, TEST

Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.

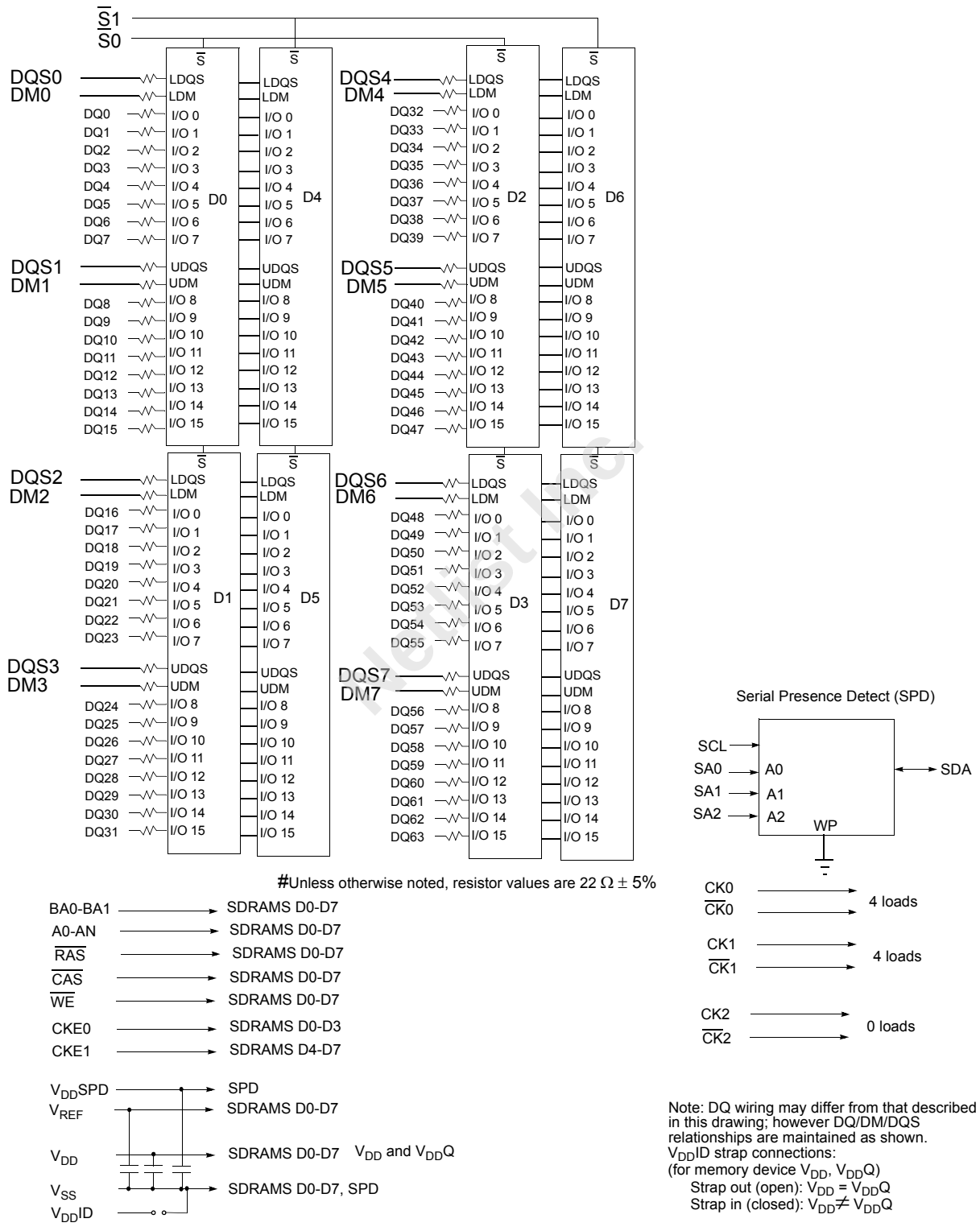
Note: Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.

Note: Pins 89, 91are reserved for x72 modules or registered modules.

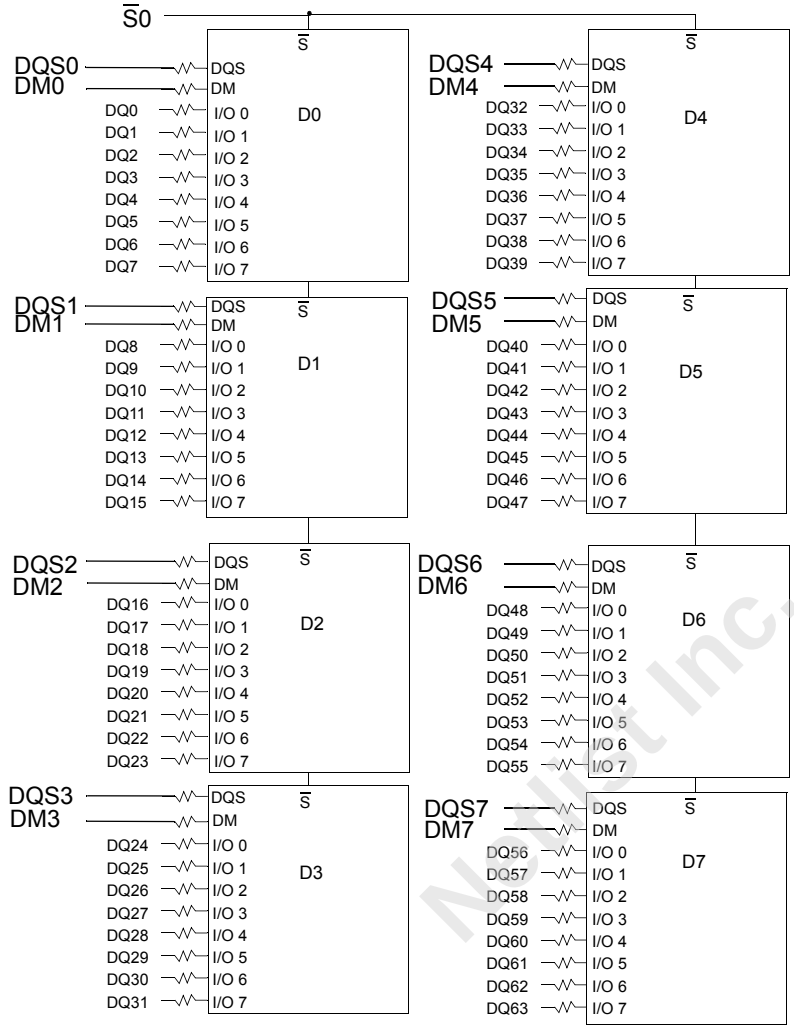
Block Diagram: Raw Card Version C (Populated as 1 physical bank of x16 SDRAMs)



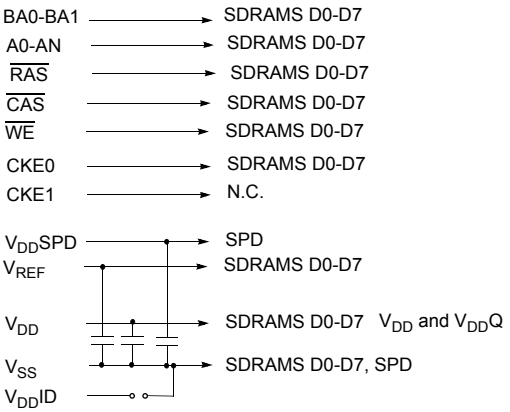
Block Diagram: Raw Card Version A (Populated as 2 physical banks of x16 SDRAMs)

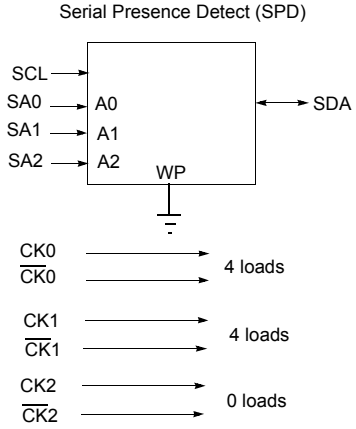


Block Diagram: Raw Card Version B (Populated as 1 physical bank of x8 SDRAMs)



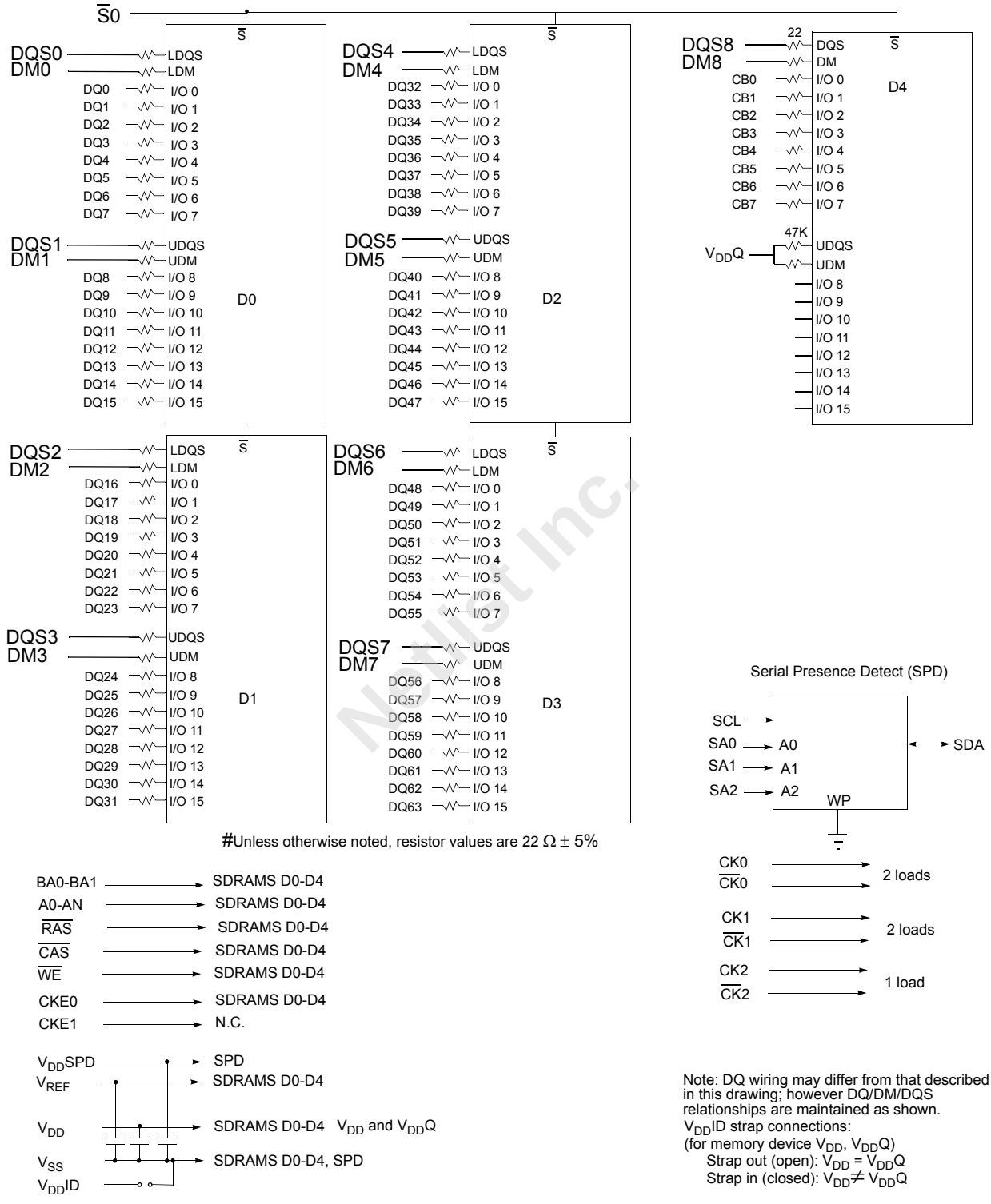
#Unless otherwise noted, resistor values are 22 Ω ± 5%





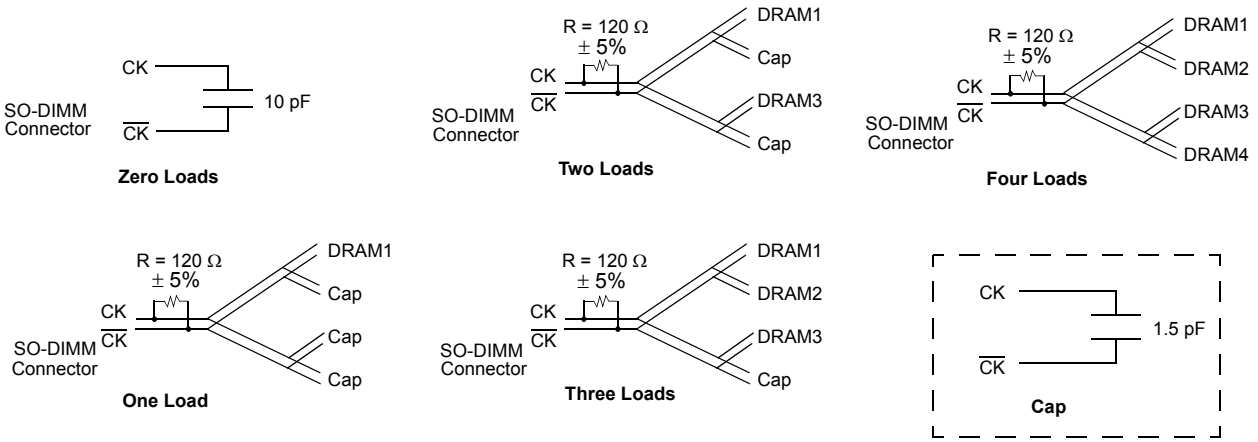
Note: DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
V_{DD}ID strap connections:
(for memory device V_{DD}, V_{DD}Q)
Strap out (open): $V_{DD} = V_{DD}Q$
Strap in (closed): $V_{DD} \neq V_{DD}Q$

Block Diagram: Raw Card Version C (Populated as 1 physical bank of x16 SDRAMs and 1 x16 SDRAM)

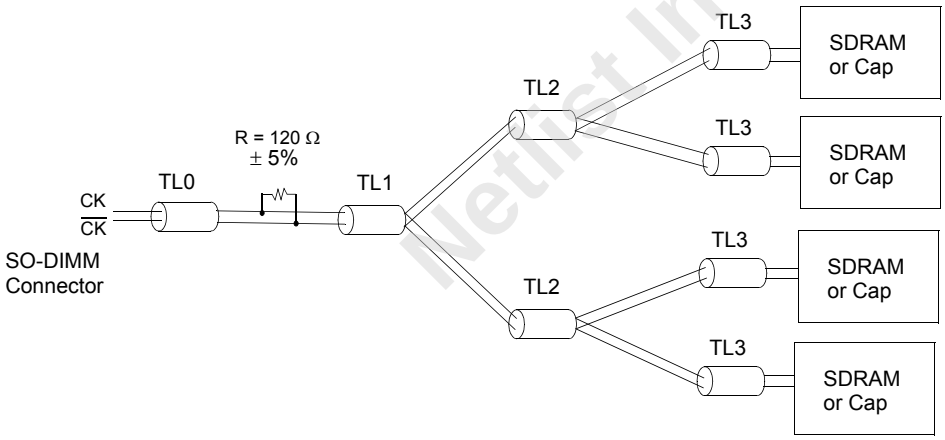


Note: DQ wiring may differ from that described in this drawing; however DQ/DM/DQS relationships are maintained as shown.
V_{DD}ID strap connections:
(for memory device V_{DD}, V_{DD}Q)
Strap out (open): $V_{DD} = V_{DD}Q$
Strap in (closed): $V_{DD} \neq V_{DD}Q$

Logical Clock Net Structures



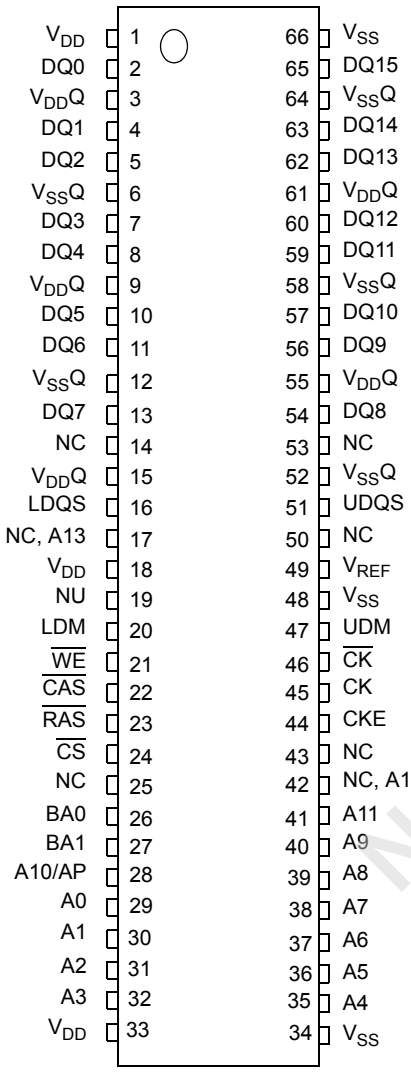
Clock Net Wiring



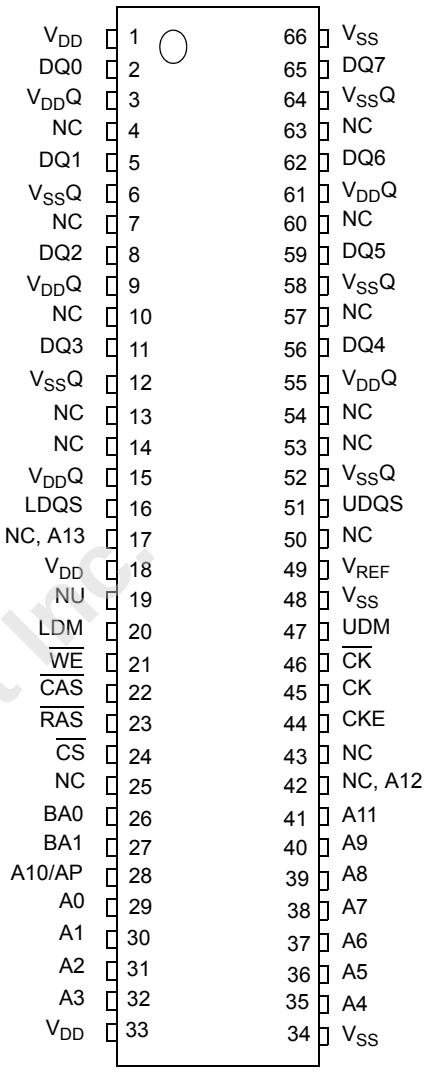
Clock Routing Trace Lengths:

Segment	TL0		TL1		TL2		TL3	
Raw Card	Min	Max	Min	Max	Min	Max	Min	Max
A, B	0.15	0.16	0.05	0.06	0.82	0.83	0.32	0.33
C	0.15	0.16	0.04	0.05	0.81	0.82	0.32	0.33

Pin Assignments for 66 pin DDR SDRAM Planar Components (Top View)



66-pin Plastic
TSOP(II) 400 mil



66-pin Plastic
TSOP(II) 400 mil

Notes:
A13 is not used on device densities below 1 Gb
A12 is not used on device densities below 256 Mb
Raw Card Versions 'A' through 'C' support the use of the above DDR SDRAM pin assignments.
These pin assignments are consistent with the JEDEC standard package definition. See JESD-79.

Reference DDR SDRAM Component Specifications

The DDR SDRAM components used with this SO-DIMM design specification are intended to be consistent with the latest revision of the JEDEC DDR400, DDR333, DDR266 and DDR200 SDRAM specifications. Refer to standard JESD-79 for component details.

Reference SPD Component Specifications

The Serial Presence Detect EEPROMs have their own power pin, V_{DD}SPD, so that they can be programmed or read without powering up the rest of the module. The wide voltage range permits use with 2.5V or 3.3V serial buses.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
V_{DD}SPD	Core Supply Voltage	2.3	3.6	V

PC3200/PC2700/PC2100/PC1600 Gerber Releases

Reference design file updates will be released as needed. This specification will reflect the most recent design files, but may be updated to reflect clarifications to the specification only; in these cases, the design files will not be updated. The following table outlines the most recent design file releases:

Raw Card	Gerber Revision	Applicable design file	Notes
A	TBD	A0	Released TBD
B	TBD	B0	Released TBD
C	TBD	C0	Released TBD

4. Unbuffered SO-DIMM Details

DDR SDRAM Module Configurations (Reference Designs)

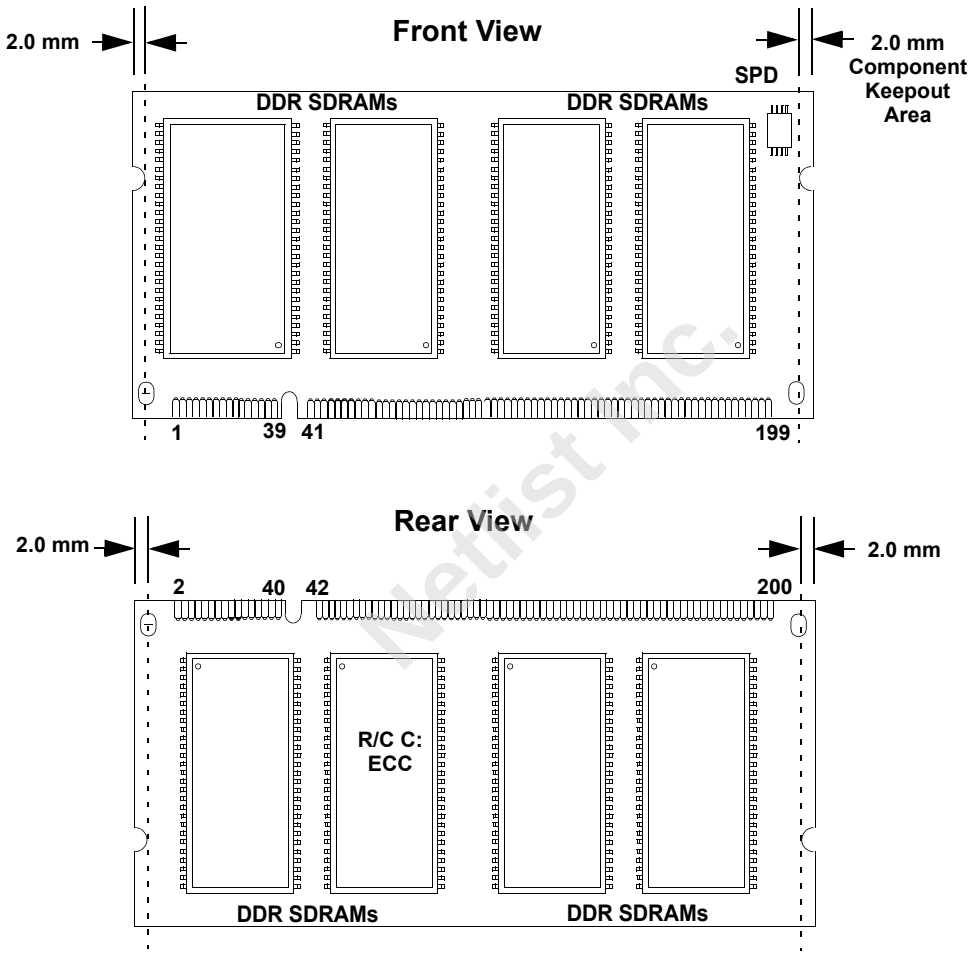
Raw Card Version	SO-DIMM Capacity	SO-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
A	64 MB	8 M x 64	64 Mbit	4 M x 16	8	66 lead TSOP	2	4	12/8
A	128 MB	16 M x 64	128 Mbit	8 M x 16	8	66 lead TSOP	2	4	12/9
A	256 MB	32 M x 64	256 Mbit	16 M x 16	8	66 lead TSOP	2	4	13/9
A	512 MB	64 M x 64	512 Mbit	32 M x 16	8	66 lead TSOP	2	4	13/10
A	1 GB	128 M x64	1 Gbit	64 M x 16	8	66 lead TSOP	2	4	14/10

Raw Card Version	SO-DIMM Capacity	SO-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
B	64 MB	8 M x 64	64 Mbit	8 M x 8	8	66 lead TSOP	1	4	12/9
B	128 MB	16 M x 64	128 Mbit	16 M x 8	8	66 lead TSOP	1	4	12/10
B	256 MB	32 M x 64	256 Mbit	32 M x 8	8	66 lead TSOP	1	4	13/10
B	512 MB	64 M x 64	512 Mbit	64 M x 8	8	66 lead TSOP	1	4	13/11
B	1 GB	128 M x64	1 Gbit	128 M x 8	8	66 lead TSOP	1	4	14/11

Raw Card Version	SO-DIMM Capacity	SO-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
C	32 MB	4 M x 64	64 Mbit	4 M x 16	4	66 lead TSOP	1	4	12/8
C	32 MB	4 M x 72	64 Mbit	4 M x 16	5	66 lead TSOP	1	4	12/8
C	64 MB	8 M x 64	128 Mbit	8 M x 16	4	66 lead TSOP	1	4	12/9
C	64 MB	8 M x 72	128 Mbit	8 M x 16	5	66 lead TSOP	1	4	12/9
C	128 MB	16 M x 64	256 Mbit	16 M x 16	4	66 lead TSOP	1	4	13/9
C	128 MB	16 M x 72	256 Mbit	16 M x 16	5	66 lead TSOP	1	4	13/9
C	256 MB	32 M x 64	512 Mbit	32 M x 16	4	66 lead TSOP	1	4	13/10
C	256 MB	32 M x 72	512 Mbit	32 M x 16	5	66 lead TSOP	1	4	13/10
C	512 MB	64 M x 64	1 Gbit	64 M x 16	4	66 lead TSOP	1	4	14/10
C	512 MB	64 M x 72	512 Mbit	64 M x 16	5	66 lead TSOP	1	4	14/10

Example Raw Card Component Placement

The component layout for Raw Cards A, B, and C are similar. In the case of Raw Card C, only one component will be included on the rear side of the card for ECC. This example is for reference only; please refer to JEDEC standard MO-224 variation BA for details.



5. SO-DIMM Wiring Details

Signal Groups

This reference specification categorizes SDRAM timing-critical signals into seven groups whose members have identical loadings and routings. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Page
Clocks for Unbuffered SO-DIMM	CK [2:0], $\overline{CK}$ [2:0]	11
Data, Check Bits, Data Mask, Data Strobe	DQ [63:0], CB[7:0], DM[8:0], DQS[8:0]	17
Select	$\overline{CS}$ [1:0]	18
Clock Enable	CKE [1:0]	19
Address/Control	Ax, BAx, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	20

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing recommendations are as follows. Other stackups and layouts are possible that meet the electrical characteristics.

- Route all signal traces except clocks using 4 mil rules, 6 mil mimum spacing between adjacent traces.
- Route clocks as much as possible using the inner layers.
- Internal signal layers and the power plane should have a ground ring around the perimeter of the board, stitched to ground at 0.5" intervals. The ground ring should be at least 20 mils wide where layout permits, but can be reduced to 10 mils when necessary.
- No test points are required.

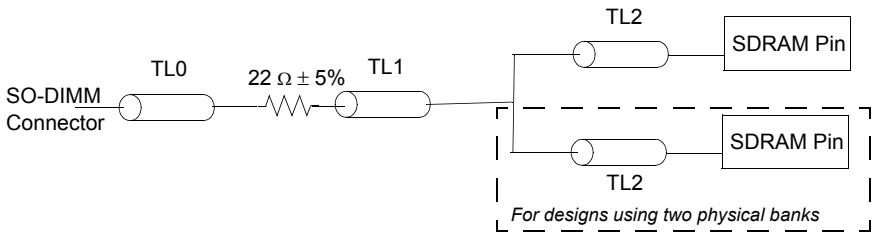
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered SO-DIMM designs. The diagrams should be used to determine individual signal wiring on a SO-DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify SO-DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one DDR SDRAM input. The net structure routing data in this document accurately represent reference Raw Card versions A, B and C.

Data Net Structures DQ[63:0], CB[7:0], DM[8:0], DQS[8:0]

Net Structure Routing for Data, Check Bits, Data Mask, Data Strobe



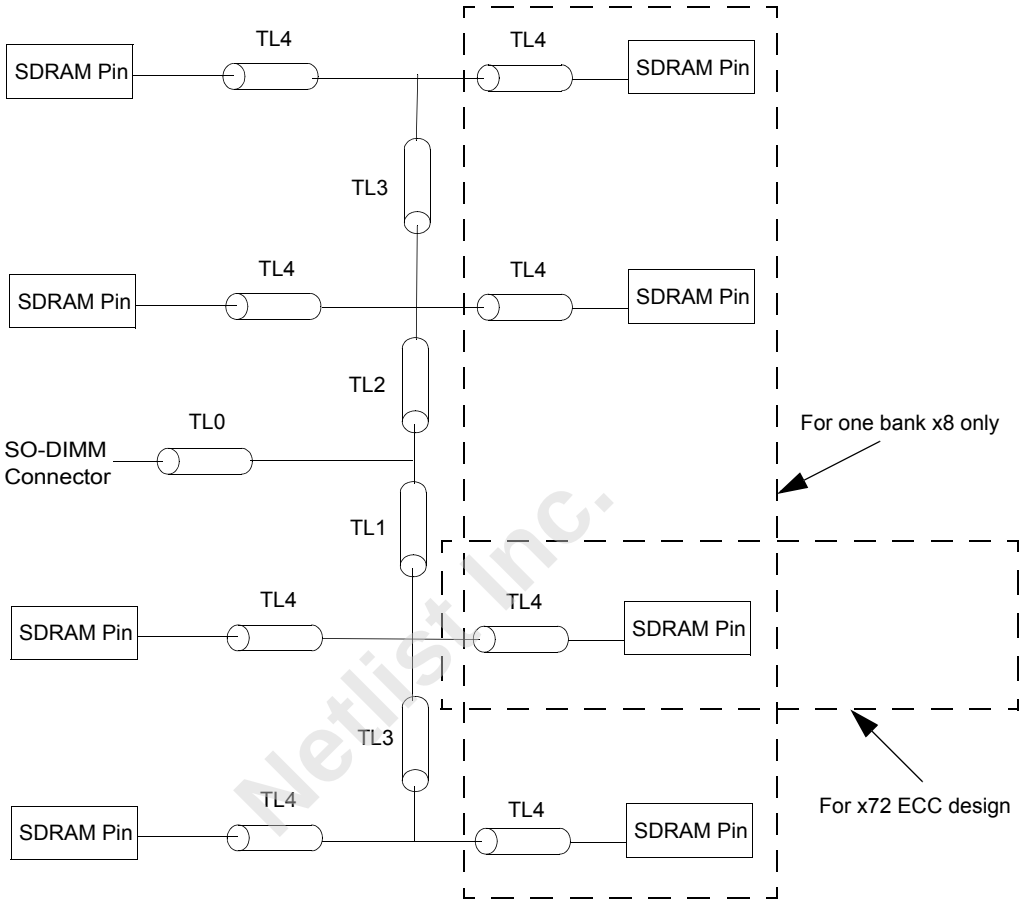
Trace Lengths for Data Net Structure

	TL0		TL1		TL2		Total	
Raw card	Min	Max	Min	Max	Min	Max	Min	Max
A	0.15	0.16	0.64	0.75	0.11	0.20	1.00	1.07
B	0.15	0.15	0.83	0.84	-	-	0.99	1.00
C	0.15	0.16	0.82	0.85	-	-	0.98	1.00

All distances are given in inches and should be kept within a tolerance of ± 0.01 inch

Select Net Structures $\overline{CS}$ [1:0]

Net Structure Routing for Select



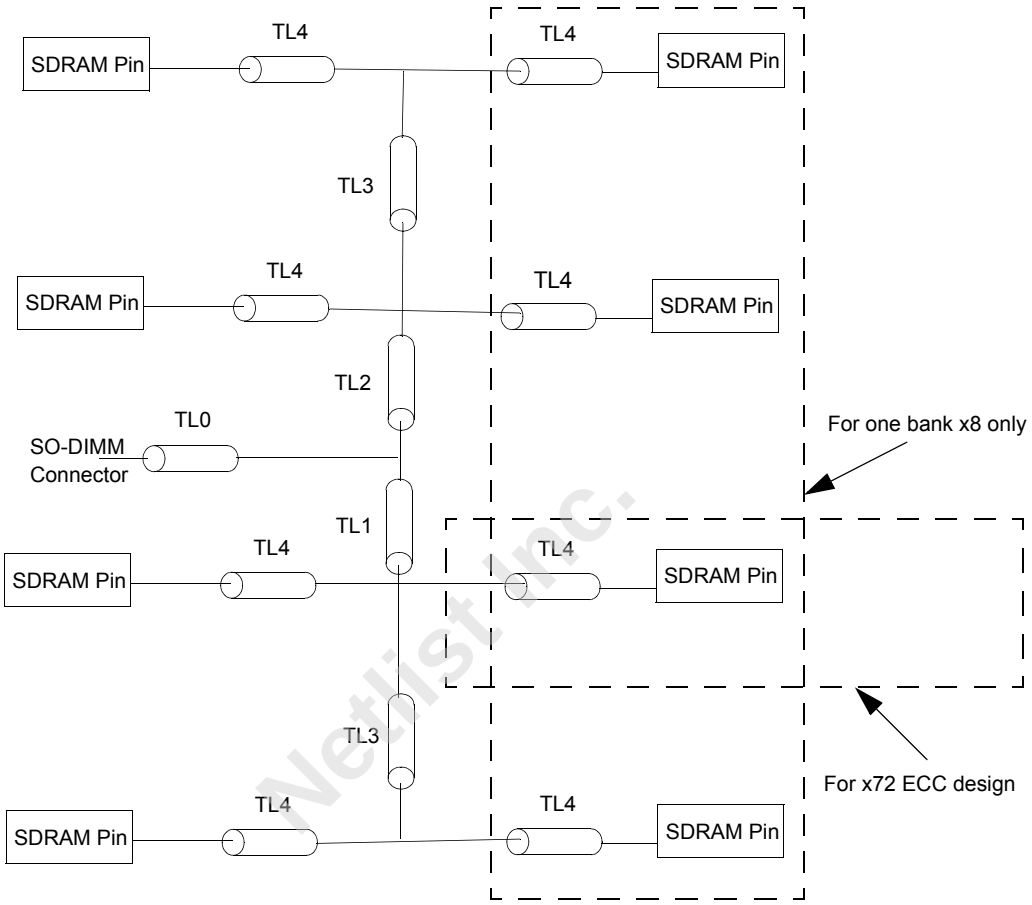
Trace Lengths for Select Net Structures

	TL0		TL1		TL2		TL3		TL4	
Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	4.01	4.01	0.43	0.45	0.43	0.45	0.60	0.60	0.14	0.20
B	1.36	1.38	0.34	0.35	0.34	0.35	0.61	0.61	0.27	0.27
C	3.48	3.49	0.39	0.40	0.39	0.40	0.56	0.57	0.26	0.27

All distances are given in inches and should be kept within a tolerance of ± 0.01 inches

Clock Enable Net Structures, CKE [1:0]

Net Structure Routing for Clock Enable



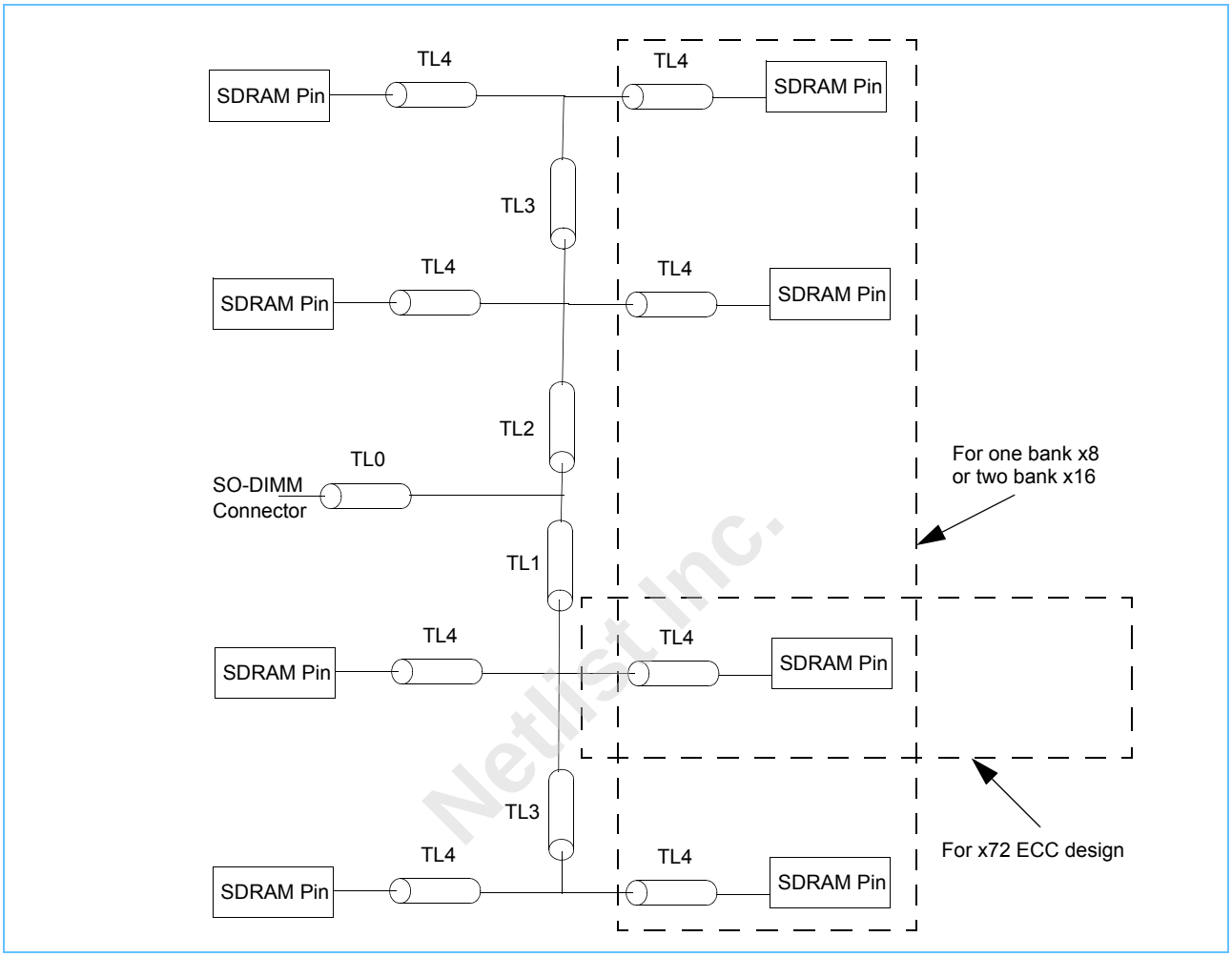
Trace Lengths for Clock Enable Net Structure

	TL0		TL1		TL2		TL3		TL4	
Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	4.01	4.02	0.43	0.45	0.43	0.45	0.60	0.60	0.14	0.20
B	1.36	1.38	0.34	0.35	0.34	0.35	0.61	0.61	0.27	0.27
C	3.48	3.49	0.39	0.40	0.39	0.40	0.56	0.57	0.26	0.27

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Address/Control Net Structures Ax, BAx, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Net Structure Routing for Address and Control



Trace Lengths for Address and Control Net Structures

	TL0		TL1		TL2		TL3		TL4	
Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A, B	1.46	1.50	0.33	0.35	0.33	0.35	0.61	0.61	0.25	0.27
C	2.89	2.90	0.35	0.36	0.47	0.48	0.56	0.57	0.26	0.27

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

Cross Section Recommendations

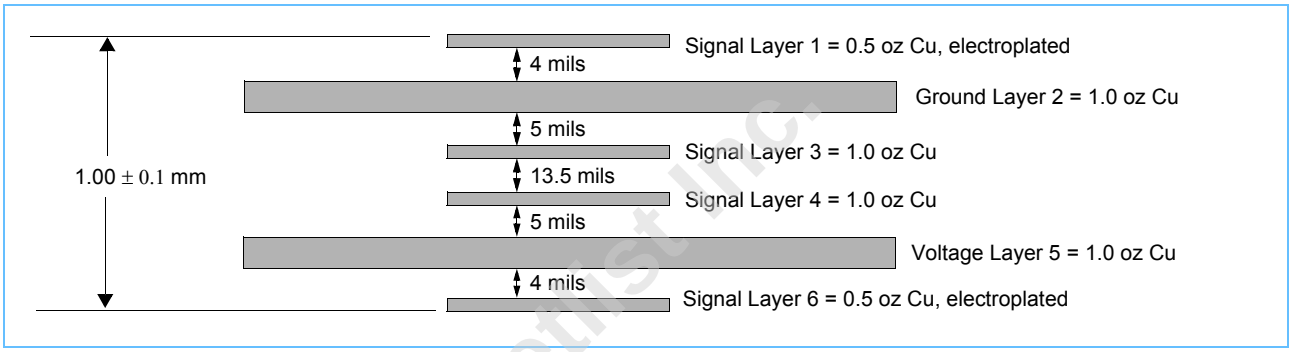
The DDR SO-DIMM printed circuit board design uses six-layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 4 mil wide traces with 6 mil spacing. The required board impedance is 60 Ω ± 10%.

Note: The PCB edge connector contacts shall be gold-plated; chamfered edges are optional.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	1.6	2.0	ns/ft
Trace velocity: S0 (inner layers)	2.0	2.2	ns/ft
Trace impedance: Z0 (all layers)	54	66	Ohms

Example Layer Stackup



Component Types and Placement

Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors, for DDR SDRAM devices, must be practically located near the device power pins.

Reference Voltage Vias

A minimum of two vias located near the connector pins should be used to connect V_{REF} to its inner routing layer.

6. Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the PC3200/PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR SDRAM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of a typical PC3200/PC2700/PC2100/PC1600 SO-DIMM. SPD values indicating different SO-DIMM performance characteristics will be utilized based on specific characteristics of the SDRAMs or SO-DIMMs. This example assumes:

- Module Organization: 16 M x 64 (128 Mbyte)
- Device Composition: 2 M x 16 bits x 4 banks (128 Mbit)
- Device Package: 66 pin TSOP-II
- Module Physical Banks: 2
- Refresh: 4 K in 64 ms

Serial Presence Detect Data Example (Part 1 of 3)

Byte #	Description	SPD Entry Value				Serial PD Data Entry (Hexadecimal)				Notes
		DDR 400	DDR 333	DDR 266A	DDR 266B	DDR 400	DDR 333	DDR 266A	DDR 266B	
0	Number of Serial PD Bytes Written during Production	128 bytes				80				
1	Total Number of Bytes in Serial PD device	256 bytes				08				
2	Fundamental Memory Type	DDR SDRAM				07				
3	Number of Row Addresses on Assembly	12				0C				
4	Number of Column Addresses on Assembly	9				09				
5	Number of MicroDIMM Banks	2				02				
6	Data Width of Assembly	64 bits				40				
7	Data Width of Assembly (continued)	64 bits				00				
8	Assembly Voltage Interface Levels ($V_{DD}Q$)	SSTL_2				04				
9	SDRAM Device Cycle Time at CL = 3.0 (t_{CK})	5.0 ns	6.0 ns	7.5 ns	7.5 ns	50	60	75	75	1
10	SDRAM Device Access Time from Clock (t_{AC})	0.70 ns	0.70 ns	0.75 ns	0.75 ns	70	70	75	75	1
11	Assembly Error Detection/Correction Scheme	Non-parity, non-ECC				00				
12	Assembly Refresh Rate/Type	15.6 µs Self Refresh				80				
13	SDRAM Device Width	x 16				10				
14	Error Checking SDRAM Device Width	Not used				00				
15	Minimum CK Delay, Random Col Access (t_{CCD})	1 clock				01				
16	Burst Lengths Supported	2, 4, 8				0E				
17	Number of Device Banks	4				04				

1. Minimum application clock cycle time is 5 ns (200 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ‘ 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ‘ 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. Unused bytes are set to the value "00".
7. Unused bits in attribute bytes are set to "0".
8. Values dependent on package type (TSOP-II or FBGA)

Serial Presence Detect Data Example (Part 2 of 3)

Byte #	Description	SPD Entry Value				Serial PD Data Entry (Hexadecimal)				Notes
		DDR 400	DDR 333	DDR 266A	DDR 266B	DDR 400	DDR 333	DDR 266A	DDR 266B	
18	$\overline{\text{CAS}}$ Latency	3,2.5,2				1C				
19	$\overline{\text{CS}}$ Latency	0 clocks				01				
20	$\overline{\text{WE}}$ Latency	1 clock				02				
21	SDRAM Module Attributes	Differential clocks				20				7
22	General SDRAM Device Attributes	Weak drivers				31				7
23	Minimum Clock Cycle at CL = 2.5 (t_{CK})	6 ns	7.5 ns	7.5 ns	10 ns	60	75	75	A0	1
24	Maximum Data Access Time (t_{AC}) from Clock at CL = 2.5	0.70 ns	0.70 ns	0.75 ns	0.75 ns	70	70	75	75	1
25	Minimum Clock Cycle Time at CL = 2.0 (t_{CK})	7.5 ns	N/A			75	N/A			6
26	Maximum Data Access Time (t_{AC}) from Clock at CL = 2.0	0.7 ns	N/A			70	N/A			6
27	Minimum Row Precharge Time (t_{RP})	18 ns				48				
28	Minimum Row Active to Row Active delay (t_{RRD})	10 ns				28				
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t_{RCD})	18 ns				48				
30	Minimum Active to Precharge Time (t_{RAS})	40 ns	42 ns	45 ns	45 ns	28	2A	2D	2D	
31	Module Physical Bank Density	64 MB				10				
32	Address and Command Setup Time Before Clock (t_{IS})	0.6 ns	0.75 ns	0.9 ns	0.9 ns	60	75	90	90	
33	Address and Command Hold Time After Clock (t_{IH})	0.6 ns	0.75 ns	0.9 ns	0.9 ns	60	75	90	90	
34	Data Input and Mask Setup Time Before Clock (t_{DS})	0.45 ns	0.45 ns	0.5 ns	0.5 ns	45	45	50	50	
35	Data Input and Mask Hold Time After Clock (t_{DH})	0.45 ns	0.45 ns	0.5 ns	0.5 ns	45	45	50	50	
36 - 40	Superset information	No superset				00				6
41	Row cycle time (t_{RC})	60 ns	60 ns	65 ns	70 ns	3C	3C	41	46	
42	Auto Refresh cycle time (t_{RFC})	70 ns	72 ns	75 ns	80 ns	46	48	4B	50	
43	Maximum SDRAM device cycle time (t_{CK}max)	8 ns	12 ns	12 ns	12 ns	20	30	30	30	
44	DQS-DQ Skew (t_{DQSQ})	0.4 ns	0.45 ns	0.50 ns	0.60 ns	28	2D	32	3C	8
45	SDRAM Device Data Hold Skew Factor (t_{QHS})	0.5 ns	0.55 ns	0.75 ns	1.0 ns	50	55	75	A0	8
46-61	Reserved		0	0	0		00	00	00	
62	SPD Revision	JEDEC 0				00				
63	Checksum for bytes 0 - 62	Calculated value				cc	cc	cc	cc	2

1. Minimum application clock cycle time is 5 ns (200 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ‘ 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ‘ 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. Unused bytes are set to the value "00".
7. Unused bits in attribute bytes are set to "0".
8. Values dependent on package type (TSOP-II or FBGA)

Serial Presence Detect Data Example (Part 3 of 3)

Byte #	Description	SPD Entry Value				Serial PD Data Entry (Hexadecimal)				Notes
		DDR 400	DDR 333	DDR 266A	DDR 266B	DDR 400	DDR 333	DDR 266A	DDR 266B	
64 - 71	Manufacturers' JEDEC ID Code									6
72	Assembly Manufacturing Location									6
73 - 90	Module Part Number									6
91 - 92	Module Revision Code									6
93 - 94	Module Manufacturing Date									3, 4
95 - 98	Module Serial Number									5
99 - 127	Manufacturer's Specific Data									6
128 - 255	Open for Customer Use	Undefined				00				

1. Minimum application clock cycle time is 5 ns (200 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. Unused bytes are set to the value "00".
7. Unused bits in attribute bytes are set to "0".
8. Values dependent on package type (TSOP-II or FBGA)

9.0 Product Label

The following label should be applied to all PC3200, PC2700, PC2100, or PC1600-compatible DDR SO-DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

Format:

PC3200m-aabc-d-ef

PC2700m-aabc-d-ef

PC2100m-aabc-d-ef

PC1600m-aabc-d-ef

Where:

m: Module Type
- S = Unbuffered DDR SO-DIMM (no registers or PLLs on module)

aa: DDR SDRAM CAS Latency
- 30 = CAS Latency 3.0
- 20 = CAS Latency 2.0
- 25 = CAS Latency 2.5

b: DDR SDRAM minimum t_{RCD} specification (in clocks)

c: DDR SDRAM minimum t_{RP} specification (in clocks)

d: JEDEC SPD Revision used on this DDR SO-DIMM
- 0 = JEDEC SPD revision 0

e: Gerber file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- C = Reference design for raw card 'C' is used for this assembly
- Z = None of the 'Reference" designs were used for this assembly

f: Revision number of the reference design used
- 1 = 1st revision
- 2 = 2nd revision

Blank = Not applicable (used with 'Z' above)

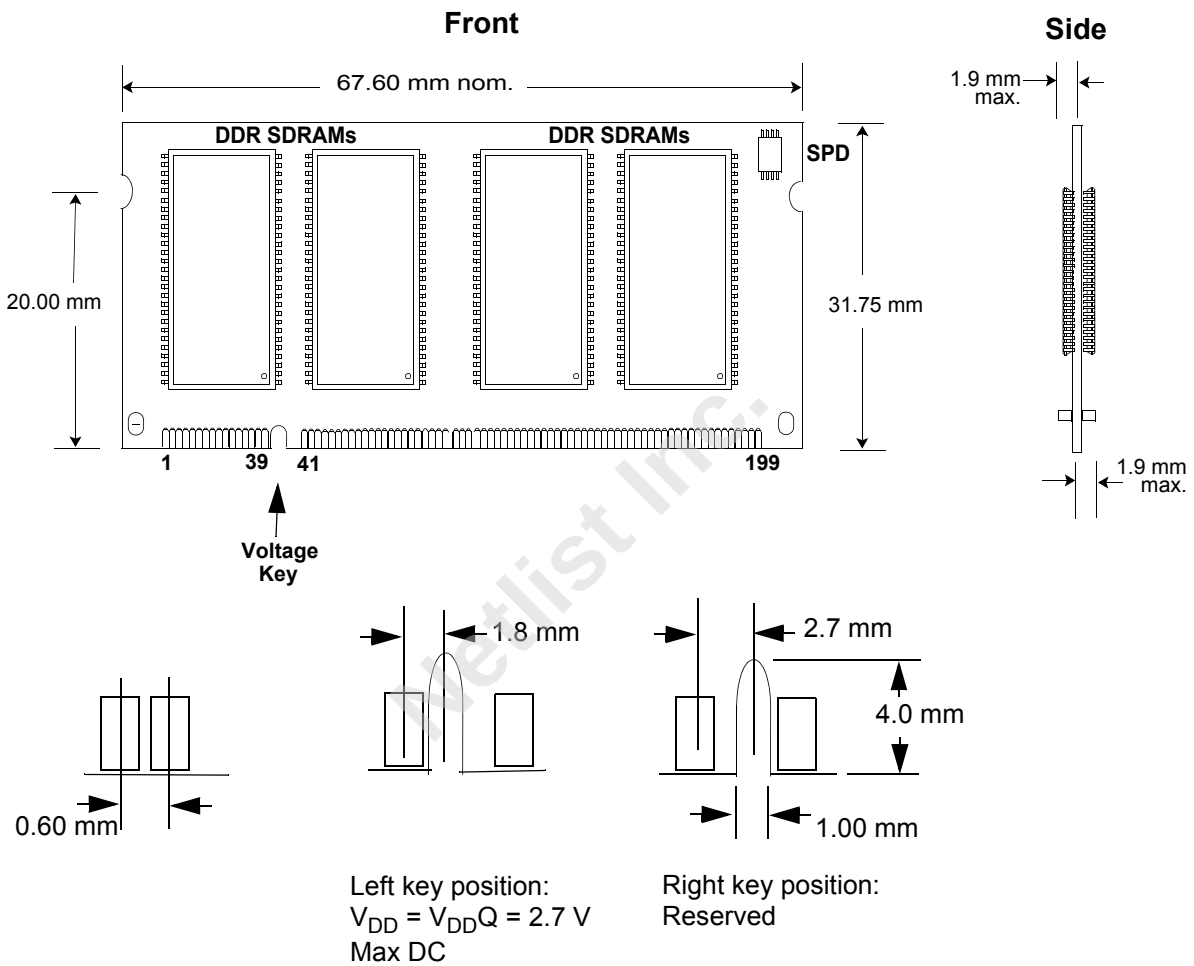
Example:

PC3200S-3033-2-B2
- is a PC3200 Unbuffered DDR SO-DIMM
- with CAS Latency = 3.0, t_{RCD} = 3, t_{RP} = 3,
- using JEDEC SPD revision 2
- and produced based on the raw card 'B' Gerber, 2nd release

7. SO-DIMM Mechanical Specifications

JEDEC has standardizing the detailed mechanical information for the 200 Pin DDR SO-DIMM family. This example is for reference only; please refer to JEDEC standard MO-224 variation BA for details.

Reference Simplified Mechanical Drawing with Keying Position



Revision History:

Date	Rev.	Changes
1/10/2003	1.4	Editorial chages from committee ballots on pages: 3,13,27
12/12/2002	1.3	Added PC3200 DIMM Support with appropriate editorial changes
5/2/2002	1.2	Added A13 for support of 1 Gbit DDR SDRAMs. Added TEST pin.
4/26/2002	1.1	Qualified design for PC2700/PC2100/PC1600. Note that pin reserved for A13 moved to match the PC2700 DDR DIMM pinout.
8/20/2001	1.0	Initial JEDEC approved release for PC2100/PC1600.